# Self-Commissioning of Inverter Dead-Time Compensation by Multiple Linear Regression Based on a Physical Model

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***Abstract*–Dead-times and switch voltage drops represent the most important sources of distortion of the (average) output voltage in PWM inverters. Their effect is a function of the parameters of the drive system and of the operating conditions, and is often intolerable in many drives applications, thus requiring a proper compensation strategy. Many techniques are implemented in industrial drives and reported in literature, even very recently. Differently from standard approaches the proposed methodology is based on a detailed physical model of the power converter (including output capacitance), described by a small set of parameters. A novel self-commissioning identification procedure is introduced, adopting Multiple Linear Regression. The technique is tested on a commercial drive in comparison to state-of-the-art techniques. Also back-EMF estimation improvements in a PMSM sensorless drive system are shown to provide additional validation of the method.**

LIST OF SYMBOLS

| | |
|---|---|
| $T_{SW}$ | switching period |
| $T_{DT}$ | dead-time duration |
| $V_{DC}$ | DC-bus voltage |
| $\delta_x$ | duty-cycle of phase $x$ $(A\ or\ B\ or\ C)$ |
| $V_{diode}$ | diode conduction voltage drop |
| $V_{IGBT}$ | IGBT conduction voltage drop |
| $V_{SW}$ | average switch voltage drop |
| $\Delta V$ | IGBT vs. diode voltage drop diff. |
| $R_s$ | motor phase resistance |
| $C_{out}$ | inverter phase output capacitance |
| $I_x$ | phase current |
| $V_{x0}$ | inverter leg voltage (referred to inverter negative terminal) |
| $V_{x0_{cap}}$ | inverter leg distortion voltage, capacitive effect |
| $V_{x0_{DT}}$ | inverter leg distortion voltage |
| $V_{xn}$ | motor phase voltage |
| $V_{xn_{DT}}$ | motor phase distortion voltage |
| $I_{thr}$ | "low" to "high" current threshold |
| $T_{delay,\mathrm{H}\to L}$ | turn-off switching delay |
| $T_{delay,\mathrm{L}\to H}$ | turn-on switching delay |
| $\chi = [\chi_0, \chi_1, \chi_2]^T$ | linear coefficients of MLR |
| $x, y$ | measured data for MLR |
| $V_{a_1}, \dots, V_{a_n}$ | voltage sampled values for MLR |
| $I_{a_1}, \dots, I_{a_n}$ | current sampled values for MLR |
| $\bar{}$ | average in the switching period |
| $\hat{}$ | estimated quantity |

## I. INTRODUCTION

Accurate compensation of inverter distortion is very important in many industrial applications of drive systems, e.g. precision servo drives, but becomes also essential in sensorless control, as voltage distortion has strong effects on the performance of the estimation technique, especially at low speed, where the operating voltage of the machine is comparable to the level of distortion. Many techniques have been proposed in the past and also very recently, [1]-[15].

Since it can be shown that phase distortion voltage depends mainly on phase current, most compensation techniques adopt a certain curve to approximate the distortion characteristic. The simplest model for dead-time effect considers diode clamping only, and results in a compensation curve that simply depends on current flow direction, [12]. Compensation, in this case, can be applied e.g. by introducing a proper modification of the PWM pulses width, in order to correct the resulting average voltage, [5]. With these simple models, a reduction of distortion is achieved, but still unsatisfactory, especially considering the increased possibilities brought by the introduction of ever faster digital signal processors. Thus, during the latest years, more complex models have been adopted, such as those using various correction functions, e.g. linear-saturated, [6], sigmoid, [9] and exponential, [7]. Moreover, in [8] the values of the distortion voltage vs. phase current curve have been stored in a look-up table (LUT), to be interpolated on-line.

The mentioned approaches require identification of parameters of the correction functions or filling-up LUT. In some cases this task is performed off-line within a self-commissioning procedure, [6][8]. Motor is normally connected to the inverter output, while different values of DC voltage or current are imposed, aiming at testing the entire current operating range. Finally data is acquired and/or processed to obtain distortion curve parameters or LUT values.

On the other hand, some methods [2][6][7][14] adapt parameters relying on the on-line measurement of harmonic distortion, or a closed-loop compensation is operated to compensate a certain harmonic (mainly the 6$^{th}$ in the rotor reference frame), [13]. Stability and influence of other sources of distortion (e.g. spatial harmonics of the air gap flux) have not been addressed yet.

Finally some compensation strategies are based on the

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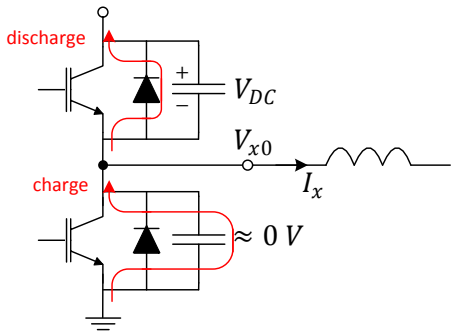



Fig. 1. Charging and discharging switch capacitance during lower IGBT switching off.

measurement of the actual phase voltage at a high sampling rate, [4], in order to obtain the actual average value in the switching period and provide a means of pre-distortion of the reference voltages before PWM modulation.

These methods have in common the lack of a physical model underlying the adopted compensation curve, being an approximation of actual phenomena occurring in the inverter.

The methodology considered in this paper, on the other hand, is based on a detailed physical model of the power converter. The distortion voltage is described by a non-linear function of current, whose parameters correspond to the actual dead-time interval, switch output capacitance, switching period and DC bus voltage, [2]. Compensation according to this model is relatively simple, once the parameters of the model are identified, and achieved results are extremely accurate.

Differently from the approach adopted in [2], where an approximation to a straight line was introduced for parameters estimation, in this case Multiple Linear Regression (MLR) is exploited, achieving a better curve fitting for distortion and resistance voltage, and finally providing a higher accuracy compensation of the inverter non-linear behavior. The validity and effectiveness of the proposal is verified on a commercial industrial drive system, by comparison to standard identification and recently introduced identification and compensation techniques. Results are firstly reported for an induction motor driven in voltage open-loop and current closed-loop control, showing the improvements introduced. The comparison among different compensation strategies is also extended by evaluating the performances of a PMSM sensorless control of a based on back-EMF observer, [17]. The results prove that the proposal provides a reduction of noise on the estimates.

## II. Accurate Modeling of Inverter Distortion

The inverter output voltage characteristics are influenced by the non-ideal behavior of the commutation phenomena, such as dead-time effect, commutation delays, voltage drops in power devices, equivalent parasitic resistance and inductance of the current paths, charging and discharging of the equivalent (parasitic or intrinsic) output capacitance of the leg. For this reason the inverter instantaneous output voltage with respect to the DC bus reference level, i.e. $V_{x0}$ in Fig. 1, will be considered in the following analysis. Averaging and extension to the phase voltage of the three-phase load will be considered as a consequence. The inductive behavior of the load allows to model the leg output current as a constant value during the switching period or, at least, during the dead-time intervals, as it will be explained shortly.

A first model will be considered, which takes into account the recalled non-ideal conditions, but neglects the effects of the outut capacitance. Later, those effects will be introduced and a complete model obtained. The simplified version of that model represents the base for the proposed self-commissioning and compensation strategy, discussed in the next sections.

### A. *Dead-time and switch voltage drops effects*

The output voltage waveforms during dead time interval ($T_{DT}$) when considering voltage drops ($V_{IGBT}$ and $V_{diode}$) and switching delays ($T_{delay,H\to L}$ and $T_{delay,L\to H}$) are sketeched in Fig. 2. Two different cases have been considered, as a function of the sign of the output current, which affects the conduction state of the free-wheeling diodes and thus the output voltage.

The voltage difference (increase or decrease) between ideal (dashed black lines) and actual switchings (solid black lines) are highlighted by coloured areas and identified by + and – signs, meaning that the corresponding contribution respectively increases or decreases the output voltage averaged over the switching period $T_{SW}$. In the following

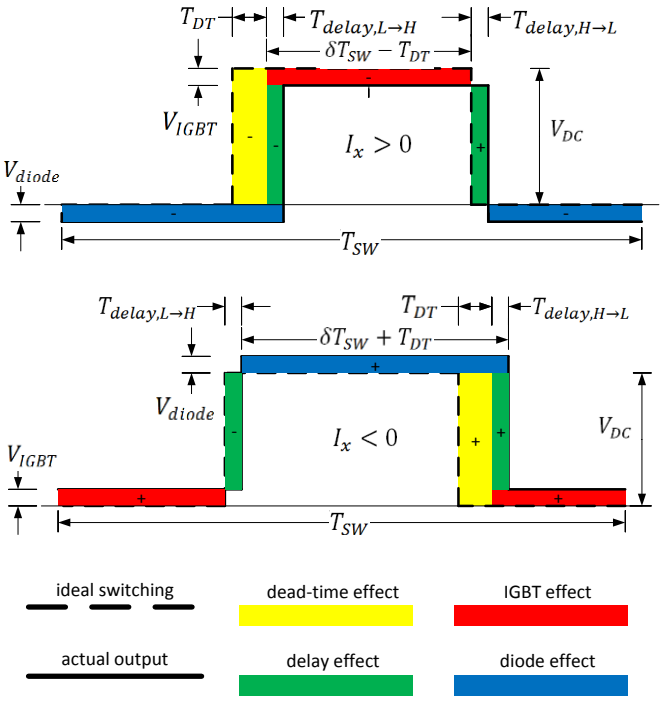



Fig. 2. Output voltage waveforms during dead time when considering voltage drops and switching delays.

sections the term $\bar{V}_{x0_{\mathrm{DT}}} = \bar{V}_{x0} - \bar{V}_{x0}^{*}$ that represents distortion of the inverter output voltage will be referred to as "distortion voltage". Symmetric commutation delays (if any) are considered with green areas, their average contribution being generally zero due to symmetry. Asymmetric commutation delays can be considered as additional dead-time components and are therefore included in that value, represented with yellow areas. Finally IGBT and diode contributions are represented with red and blue areas.

The equivalent on-time of the output voltage can be therefore related to the commanded duty cycle $\delta_x$ and the dead-time, as shown in the same figure. If the average value of the output voltage is considered within the switching period, the following equations are obtained for distortion voltage as a function of the output current sign:

$$I_x > 0: \bar{V}_{x0_{\mathrm{DT}}} = \frac{1}{T_{SW}}\left\{-\underbrace{V_{DC}T_{DT}}_{\square} - \underbrace{V_{IGBT}(\delta_x T_{SW} - T_{DT})}_{\square} - \underbrace{V_{diode}[(1-\delta_x)T_{SW} + T_{DT}]}_{\square}\right\} \quad (1)$$

$$I_x < 0: \bar{V}_{x0_{\mathrm{DT}}} = \frac{1}{T_{SW}}\left\{\underbrace{V_{DC}T_{DT}}_{\square} + \underbrace{V_{IGBT}[(1-\delta_x)T_{SW} - T_{DT}]}_{\square} - \underbrace{V_{diode}(\delta_x T_{SW} + T_{DT})}_{\square}\right\} \quad (2)$$

Previous equations can be manipulated after the introduction of the following equation relating the IGBT and diode voltage drops:

$$V_{IGBT} = V_{diode} + \Delta V \quad (3)$$

thus obtaining:

$$I_x > 0: \ \bar{V}_{x0_{\mathrm{DT}}} = -V_{DC}\frac{T_{DT}}{T_{SW}} - V_{diode} - \Delta V\left(\delta_x - \frac{T_{DT}}{T_{SW}}\right)$$
$$I_x < 0 \ : \ \bar{V}_{x0_{DT}} = V_{DC}\frac{T_{DT}}{T_{SW}} + V_{diode} + \Delta V\left(1 - \delta_x - \frac{T_{DT}}{T_{SW}}\right) \quad (4)$$

In the case of small phase voltage (i.e. $\delta_x \cong 0.5$), a first symplified equation can be obtained

$$\bar{V}_{x0_{\mathrm{DT}}} = -\mathrm{sign}(I_x)\left[V_{DC}\frac{T_{DT}}{T_{SW}} + V_{diode} + \Delta V\left(0.5 - \frac{T_{DT}}{T_{SW}}\right)\right] \quad (5)$$

If dead-time interval is small with respect to switching period, the very last term of (5) can be neglected, leading to

$$\bar{V}_{x0_{\mathrm{DT}}} = -\mathrm{sign}(I_x)\left(V_{DC}\frac{T_{DT}}{T_{SW}} + V_{diode} + 0.5\,\Delta V\right) \quad (6)$$

### B. *Introducing the effect of capacitance*

The adopted full model comprises parasitic capacitance

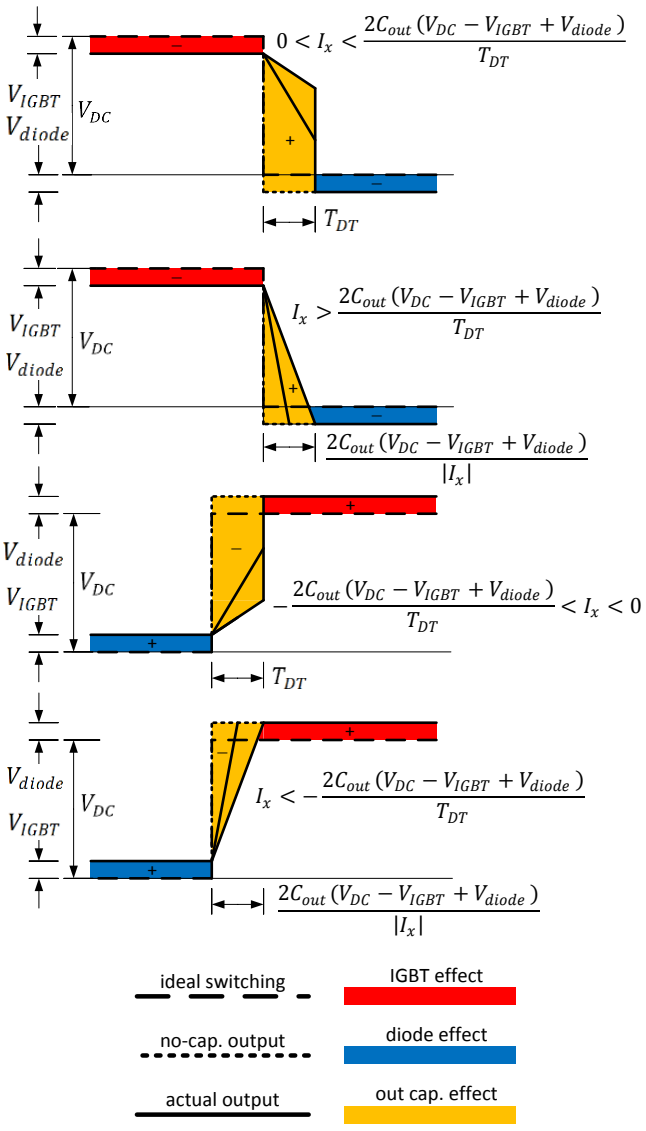



Fig. 3. Output voltage waveforms during dead time when considering output capacitance and different values of the output current.

charging effect, [1][10][15][16]. During the dead-time interval the output current tends to force a commutation due to the turn on of the opposite diode. One of the possible situations is sketched in Fig. 1, where switching off of the low-side IGBT is considered. The output current is negative (i.e. entering the output node) and initial voltage is equal to the lower IGBT voltage drop. Due to the presence of the switch capacitance, output voltage does not rise immediately, as the upper capacitance has to be discharged and lower one charged.

Four different cases can be considered as a function of the sign and the absolute value of the output current, as depicted in Fig. 3. In fact, if the time required to charge/discharge the output capacitance is higher than the dead-time interval (i.e. when the output current is quite low), the commutation is slower and a discontinuity is experienced in the output

voltage as soon as the higher IGBT switches on at the end of the dead-time interval. The limit condition between the ideal ramp transition and intermediate lower slope cases can be calculated by matching the charge and discharge time and dead-time. If the IGBT and diode voltage drops are taken into account, this results in

$$I_x = \frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}} \tag{7}$$

where $C_{out}$ is the overall output capacitance.

The difference between the areas in Fig. 2, i.e. null capacitance, and that of Fig. 3 are then considered, and four expressions are obtained as a function of the output current:

$$if \quad 0 < I_x < \frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left\{(V_{DC} - V_{IGBT} + V_{diode})T_{DT} - \frac{|I_x|}{4C_{out}}T_{DT}^2\right\} \tag{8}$$

$$if \quad I_x > \frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left\{\frac{C_{out}(V_{DC} - V_{IGBT} + V_{diode})^2}{|I_x|}\right\} \tag{9}$$

$$if \quad -\frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}} < I_x < 0$$
$$\bar{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left\{-(V_{DC} - V_{IGBT} + V_{diode})T_{DT} + \frac{|I_x|}{4C_{out}}T_{DT}^2\right\} \tag{10}$$

$$if \quad I_x < -\frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0_{cap}} = \frac{1}{T_{SW}}\left\{-\frac{C_{out}(V_{DC} - V_{IGBT} + V_{diode})^2}{|I_x|}\right\} \tag{11}$$

representing the contribution of the output capacitance to average output voltage distortion $\bar{V}_{x0}$.

Finally the two contributions, i.e. the last four equations and those calculated in (1),(2) can be joined to obtain the overall average distortion voltage in the different current conditions, as reported in the following equations:

$$if \quad 0 < I_x < \frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0} = \frac{1}{T_{SW}}\left\{V_{DC}\delta_x T_{SW} - V_{DC}T_{DT} - V_{IGBT}(\delta_x T_{SW} - T_{DT}) - V_{diode}[(1-\delta_x)T_{SW} + T_{DT}] + (V_{DC} - V_{IGBT} + V_{diode})T_{DT} - \frac{|I_x|}{4C_{out}}T_{DT}^2\right\} \tag{12}$$

$$if \quad I_x > \frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0} = \frac{1}{T_{SW}}\left\{V_{DC}\delta_x T_{SW} - V_{DC}T_{DT} - V_{IGBT}(\delta_x T_{SW} - T_{DT}) - V_{diode}[(1-\delta_x)T_{SW} + T_{DT}] + \frac{C_{out}(V_{DC} - V_{IGBT} + V_{diode})^2}{|I_x|}\right\} \tag{13}$$

$$if \quad -\frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}} < I_x < 0$$
$$\bar{V}_{x0} = \frac{1}{T_{SW}}\left\{V_{DC}\delta_x T_{SW} + V_{DC}T_{DT} + V_{IGBT}[(1-\delta_x)T_{SW} - T_{DT}] + V_{diode}(\delta_x T_{SW} + T_{DT}) - (V_{DC} - V_{IGBT} + V_{diode})T_{DT} + \frac{|I_x|}{4C_{out}}T_{DT}^2\right\} \tag{14}$$

$$if \quad I_x < -\frac{2C_{out}(V_{DC} - V_{IGBT} + V_{diode})}{T_{DT}}$$
$$\bar{V}_{x0} = \frac{1}{T_{SW}}\left\{V_{DC}\delta_x T_{SW} + V_{DC}T_{DT} + V_{IGBT}[(1-\delta_x)T_{SW} - T_{DT}] + V_{diode}(\delta_x T_{SW} + T_{DT}) - \frac{C_{out}(V_{DC} - V_{IGBT} + V_{diode})^2}{|I_x|}\right\} \tag{15}$$

## III. MODEL SIMPLIFICATION: CALCULATION OF PHASE VOLTAGE DISTORTION

The model introduced above can be greatly simplified under the following hypotheses:

- $\delta_x \approx 0.5$ (small phase voltage);
- $T_{DT} \ll \delta_x T_{SW}$ (small phase voltage and dead-time);
- $V_{IGBT} \ll V_{DC}$ (small IGBT voltage drop);
- $V_{diode} \ll V_{DC}$ (small diode voltage drop).

obtaining the following expressions for the leg output voltage:

$$if \quad |I_x| < \frac{2C_{out}V_{DC}}{T_{DT}}$$
$$\bar{V}_{x0} = V_{DC}\delta_x - \text{sign}(I_x)\,V_{SW} - \frac{T_{DT}^2}{4C_{out}T_{SW}}I_x \tag{16}$$

$$if \quad |I_x| > \frac{2C_{out}V_{DC}}{T_{DT}}$$
$$\bar{V}_{x0} = V_{DC}\delta_x - \text{sign}(I_x)\,V_{DC}\frac{T_{DT}}{T_{SW}} - \text{sign}(I_x)\,V_{SW} + \frac{C_{out}{V_{DC}}^2}{T_{SW}}\cdot\frac{1}{I_x} \tag{17}$$

The distortion voltage curve represented by this model is shown in Fig. 4. It is worth to mention that the small phase voltage condition (i.e. $\delta_x \approx 0.5$) represents indeed the situation in which inverter distortion compensation is mostly needed. Distortion voltage component can be therefore expressed as a

function of:

- three parameters, i.e. $T_{DT}$, $C_{out}$ and the average value of the two devices voltage drops $V_{SW} = \frac{V_{IGBT}+V_{diode}}{2}$;
- two variables, i.e. $I_x$ and $V_{DC}$; both are measured, the second one is slowly varying and belongs to a limited range, therefore it can be considered as a known parameter.

As it can be seen both from the above equations and in Fig. 4, the presence of output capacitance influences the shape (slope, in particular) of the distortion voltage vs. current characteristic, while the asymptotic value at high-current is proportional to $T_{DT}$.

Hereafter the distortion on phase voltage will be evaluated for a particular case, i.e. considering the injection of a controlled current space vector along the phase $a$ of the motor. As it will be shown, this situation is particularly convenient for the sake of parameters identification, and represents a significant case since standard experimental tests for dead-time distortion characteristic are normally referred to it.

Due to the particular choice of the current space vector the following trivial condition holds:

$$I_b = I_c = -I_a/2 \tag{18}$$

which allows to calculate all the voltage distortion components as a function of the same current $I_a$. Three different conditions have to be considered, i.e. the current is below (i.e. "low-current") the threshold $I_{thr} = \frac{2C_{out}V_{DC}}{T_{DT}}$, above twice the same threshold (i.e. "high-current") or intermediate:

$$if \quad |I_a| < I_{thr}$$

$$\bar{V}_{a0_{DT}} = -\text{sign}(I_a)\, V_{SW} - \frac{T_{DT}^2}{4C_{out}T_{SW}} I_a \tag{19}$$

$$\bar{V}_{b0_{DT}} = \bar{V}_{c0_{DT}} = \text{sign}(I_a)\, V_{SW} + \frac{1}{2}\frac{T_{DT}^2}{4C_{out}T_{SW}} I_a$$

$$if \quad I_{thr} < |I_a| < 2I_{thr}$$

$$\bar{V}_{a0_{DT}} = -\text{sign}(I_a)\, V_{DC}\frac{T_{DT}}{T_{SW}} - \text{sign}(I_a)\, V_{SW} + \frac{C_{out}{V_{DC}}^2}{T_{SW}} \cdot \frac{1}{I_a} \tag{20}$$

$$\bar{V}_{b0_{DT}} = \bar{V}_{c0_{DT}} = \text{sign}(I_a)\, V_{SW} + \frac{1}{2}\frac{T_{DT}^2}{4C_{out}T_{SW}} I_a$$

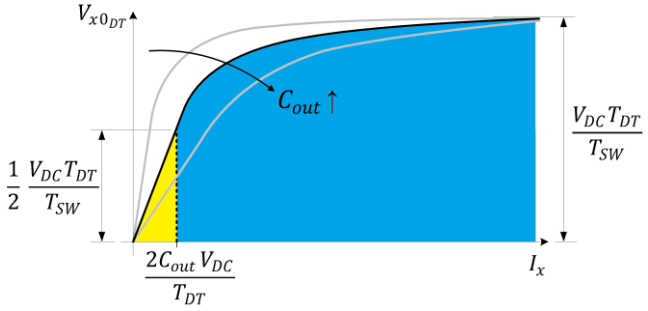



Fig. 4. Simplified curve of phase leg distortion voltage.

$$if \quad |I_a| > 2I_{thr}$$

$$\bar{V}_{a0_{DT}} = -\text{sign}(I_a)\, V_{DC}\frac{T_{DT}}{T_{SW}} - \text{sign}(I_a)\, V_{SW} + \frac{C_{out}{V_{DC}}^2}{T_{SW}} \cdot \frac{1}{I_a} \tag{21}$$

$$\bar{V}_{b0_{DT}} = \bar{V}_{c0_{DT}} = \text{sign}(I_a)\, V_{DC}\frac{T_{DT}}{T_{SW}} + \text{sign}(I_a)\, V_{SW} - \frac{C_{out}{V_{DC}}^2}{T_{SW}} \cdot \frac{2}{I_a}$$

Motor phase voltage can be finally calculated by considering a balanced condition and the relationship between inverter output leg voltage $V_{x0}$ and neutral point voltage $V_{n0}$, i.e. $V_{xn} = V_{x0} - V_{n0}$, where $V_{n0} = \frac{V_{a0}+V_{b0}+V_{c0}}{3}$.

Both for "high" and "low" currents the dependence of distortion voltage on current is quite straightforward and is similar to that of leg voltage, but in the intermediate range both the effects are in some way superimposed, meaning that a relatively accurate knowledge of the involved parameters is needed for a proper compensation. Through experimental verification it was finally highlighted that the effect of the devices voltage drops $V_{SW}$ can be neglected, [10], and previous equations can be further simplified. If a balanced resistive load (e.g. the motor windings in DC) is considered, phase voltage reference available at the output of the vector control algorithm is:

$$\bar{V}_{an}^* = \bar{V}_{an} - \hat{V}_{an_{DT}} = R_S I_a - \hat{V}_{an_{DT}} \tag{22}$$

which, according to the simplified model, becomes:

$$if \quad |I_a| < I_{thr}$$

$$\bar{V}_{an}^* = \frac{T_{DT}^2}{4C_{out}T_{SW}} I_a + R_S I_a \tag{23}$$

$$if \quad I_{thr} < |I_a| < 2I_{thr}$$

$$\bar{V}_{an}^* = \frac{2}{3}\text{sign}(I_a)\, V_{DC}\frac{T_{DT}}{T_{SW}} - \frac{2}{3}\frac{C_{out}{V_{DC}}^2}{T_{SW}} \cdot \frac{1}{I_a} + \frac{1}{3}\frac{T_{DT}^2}{4C_{out}T_{SW}} I_a + R_S I_a \tag{24}$$

$$if \quad |I_a| > 2I_{thr}$$

$$\bar{V}_{an}^* = \frac{4}{3}\text{sign}(I_a)\, V_{DC}\frac{T_{DT}}{T_{SW}} - 2\frac{C_{out}{V_{DC}}^2}{T_{SW}} \cdot \frac{1}{I_a} + R_S I_a \tag{25}$$

In Fig. 5 a graphical representation of the phase voltage reference (solid line) and its distortion component (dashed line) as a function of the output current is shown for a typical case. It can be seen that a linear-saturated model can roughly approximate the curve, since in the leftmost part of the diagram (i.e. "low" current) the dependence is linear, whilst in the rightmost part (i.e. "high" current) a constant term prevails. This also explains the conventional approaches to dead-time compensation by piece-wise linear saturated functions.

## IV. Self-Commissioning: Parameters Identification

The possibility of off-line self-identification for the dead-time distortion parameters and phase resistance was already demonstrated in [2], where a simple self-commissioning procedure, based on an approximated fitting of the phase voltage vs. current curve, was developed and tested. In that case the main approximation was related to the high-current behavior, where dead-time distortion was considered as a constant value. Based on empirical data, a certain current level had to be chosen as a threshold above which the asymptotic value was considered as reached.

Although accuracy could be satisfactory in many cases, that approach can lead to a small but non-negligible error in the identification of parameters, as it will be seen in the experimental results section of this paper. the determination of a sufficiently high current threshold is not trivial (especially if motor and inverter current limits are not matched), and measurements in a large intermediate part of the current range cannot be exploited, which results in non-optimal identification accuracy (resistance is usually over-estimated). A peculiar situation is represented by the presence of a long cable connecting inverter and motor (as it often happens in industrial applications), where a good curve fitting is difficult to achieve with that simple approach.

To overcome these issues, a self-commissioning procedure based on MLR has been developed, which exploits the whole *"high-current"* range (Fig. 5). Therefore in this proposal, based on the model of distortion described above, MLR (at "high-current"), and straight line regression (at "low"-current") are applied in order to identify off-line the actual distortion function parameters, exploiting the expressions of phase voltage (23)-(25). The same equations and the identified parameters are then used for on-line compensation. Fitting accuracy and resistance estimation are sensibly improved, since the curve at high-current is considered in its non-linear terms, rather than being approximated to a straight line. Even if the applied algorithm is relatively more complex, the increase in computational cost with respect to the previous approach has a small impact, especially considering that it has to be run off-line.

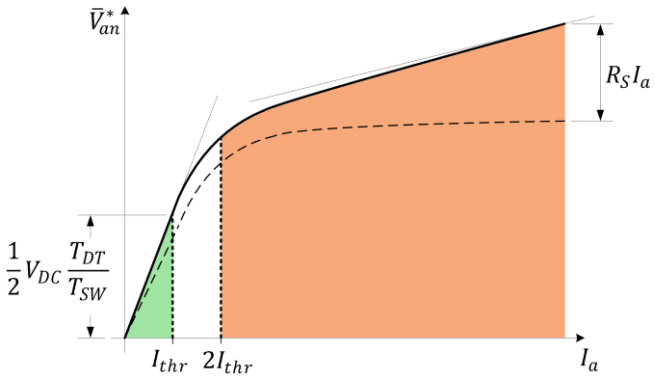



Fig. 5. Phase voltage reference vs. current curve in the commissioning conditions.

The self-commissioning procedure can be divided into two main steps: motor feeding with measurement and acquisition, followed by processing. During the first step the motor current is controlled to reach a sequence of different steady-state operating points, and the needed measurement quantities are acquired. It is worth mentioning that only the cumulative sum of current, voltage and some combinations of the two are stored (seven variables, as it will be shown hereafter), instead of all the time samples. In the second stage collected data is processed in order to calculate the compensation parameters introduced in previous sections.

### A. Feeding of the motor and data collection

The proposed test is meant to be performed at the commissioning stage, enabling only the vector current control and imposing a certain sequence of current references. Current control has of course to be tuned to guarantee stability, but its dynamical behavior is not crucial. Since phase currents are considered, knowledge of the rotor position is not required (thus the method is applicable also to sensorless systems), while rotor has to be at stand-still (for each tested operating point, shaft must not move during acquisition). As already discussed, a certain phase of the inverter will be considered, i.e. phase $a$, but the same procedure can be repeated for any of the three phases.

When dead-time distortion compensation is disabled, the voltage needed to control a certain current value comes from current regulators and, at steady-state, corresponds to the inverter distortion voltage added to the resistive drop, as in (22). If a staircase-shaped increasing current reference is imposed along one phase and controlled by the vector current regulation loop, a sequence of different DC operating points can be tested. For each step, steady-state current and voltage samples are processed. The current range for the test is chosen depending on the rated current of motor and inverter.

The acquisition range is divided into two regions, i.e. "low current" region and "high current" region, as highlighted in Fig. 5, while the medium current region will be discarded. A tentative value for the threshold is simple to find using the nominal PWM dead-time, since the resistive voltage drop can be neglected at low-current. Moreover, it has been seen experimentally that the accuracy of the ranges separation is, for the present technique, not critical to the fitting results, due to the smoothness of the curve. A priori knowledge of the output capacitance could help in the identification process, but it must be considered that this quantity is heavily influenced by power connections between inverter and motor.

A "high current" region threshold is obtained as twice the "low current" region range, and defines the current value at which the accumulation process starts. Threshold values can be expressed as a function of system parameters, i.e.

"low current" region: $I_a \leq I_{thr}$

$$\bar{V}_{an} \leq V_{thr} = \frac{1}{2} V_{DC} \frac{T_{DT}}{T_{SW}} \quad (26)$$

"high current" region: $I_a > 2I_{thr}$ (27)

Accumulation of voltage, current and combinations of the two is initially performed for each sample of the "high-current" range:

$$\sum_{i=1}^{n} V_{a_i} \cdot \text{sign}(I_{a_i}),\quad \sum_{i=1}^{n} |I_{a_i}|,\quad \sum_{i=1}^{n} V_{a_i} I_{a_i},\quad \sum_{i=1}^{n} I_{a_i}^2,\quad \sum_{i=1}^{n} \frac{1}{|I_{a_i}|},\quad \sum_{i=1}^{n} \frac{1}{I_{a_i}^2},\quad \sum_{i=1}^{n} \frac{V_{a_i}}{I_{a_i}} \quad (28)$$

*B. Calculation of compensation parameters*

Calculation of the compensation parameters is based on the accumulated values stored during the feeding and acquisition phase, (28). Current measurement offset effect can also be taken into account as an additional parameter and estimated during this procedure, exploiting the expected symmetry of the voltage vs. current characteristic.

Distortion voltage can be rewritten in analogy with (25)

$$\bar{V}_{an_{DT}} = \text{sign}(I_a) \cdot \chi_0 + \chi_1 I_a + \frac{\chi_2}{I_a} \quad (29)$$

with generic coefficients $\chi_{0,1,2}$:

$$\chi_0 = \frac{4}{3} V_{DC} \frac{T_{DT}}{T_{SW}},\quad \chi_1 = R_S,\quad \chi_2 = -2 \frac{C_{out} {V_{DC}}^2}{T_{SW}} \quad (30)$$

After having defined appropriate vector quantities

$$x = \begin{bmatrix} \text{sign}(I_{a_1}) & I_{a_1} & \frac{1}{I_{a_1}} \\ \cdots & \cdots & \cdots \\ \text{sign}(I_{a_n}) & I_{a_n} & \frac{1}{I_{a_n}} \end{bmatrix},\quad y = \begin{bmatrix} V_{a_1} \\ \cdots \\ V_{a_n} \end{bmatrix},\quad \chi = \begin{bmatrix} \chi_0 \\ \chi_1 \\ \chi_2 \end{bmatrix} \quad (31)$$

where $n$ is the number of acquired samples, the least squares estimate for the coefficients vector $\chi$ will be obtained by means of Multiple Linear Regression:

$$\hat{\chi} = (x^T x)^{-1} x^T y \quad (32)$$

Evaluation of this expression is done by using data stored in the accumulators (28). Finally, by simple manipulation of (30), distortion parameters and resistance are estimated from the identified coefficients $\hat{\chi}$. A flow-chart of the identification procedure is summarized in Fig. 6.

Current sensor accuracy is of course important during identification, as in most motor control issues. However, as it will be shown in the next section, the procedure was successfully implemented and tested on commercial hardware, with simple software modifications, demonstrating its robustness in real-world conditions. Since the measurements are taken at steady-state, high-frequency noise can be easily rejected by low-pass filtering.

The self-commissioning can include a standard sensor offset estimation sequence right before its start. Moreover, elimination of the DC offset can be obtained by exploiting symmetry, as mentioned above, or by using the intercept value obtained by straight-line regression in the low-current range.

During on-line compensation, the current measurement offset represents an important issue, which can cause the presence of a sensible DC voltage, [18]. However, this represents a general issue related to dead-time distortion, not related in particular to the proposed technique.

An alternative estimation of one of the parameters (e.g. to increasing accuracy or robustness of the identification) can be obtained from the low-current expression (23), exploiting the values estimated at high current.

## V. Experimental results

The complete hardware of an industrial drive has been used for experimental investigation, in order to confirm the correctness of the theoretical approach and to show the effectiveness of the proposed compensation and self-commissioning proposal, [2].

A Gefran ADL200 commercial drive has been used for the experimental tests, with original hardware and partially modified control software. The control update and PWM switching is operated at 10 kHz. Since the inverter IGBT module is oversized with respect to the continuous-duty rating for reliability reasons, the inverter command interlock time is relatively large, i.e. 2.5 μs. Considering the nominal DC bus voltage (565 V, i.e. the rectified three-phase 400V grid voltage), this results in a theoretical maximum phase voltage distortion which saturates at about 19 V for large currents.

The distortion problem could be attenuated in some small-power inverters, where the interlock time can be significantly reduced. However these cases the switching

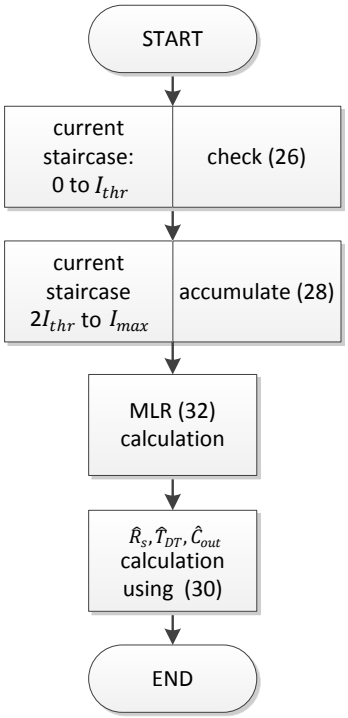



Fig. 6. Flow-chart of the self-commissioning identification procedure.

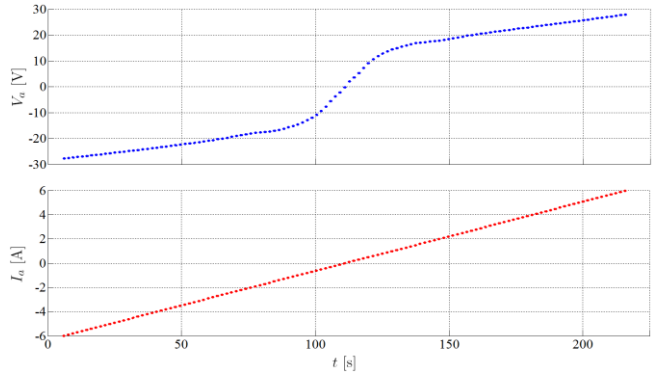
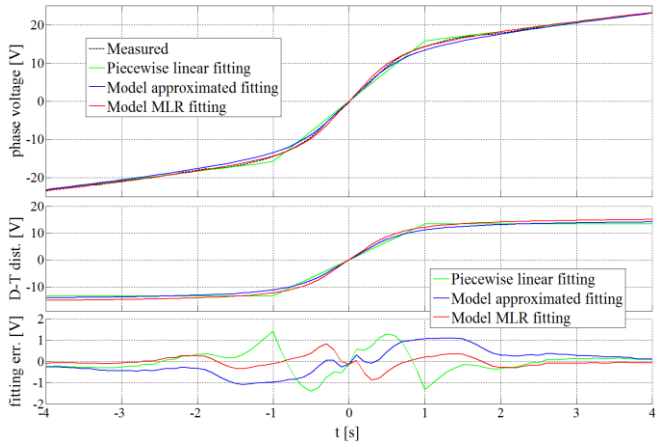
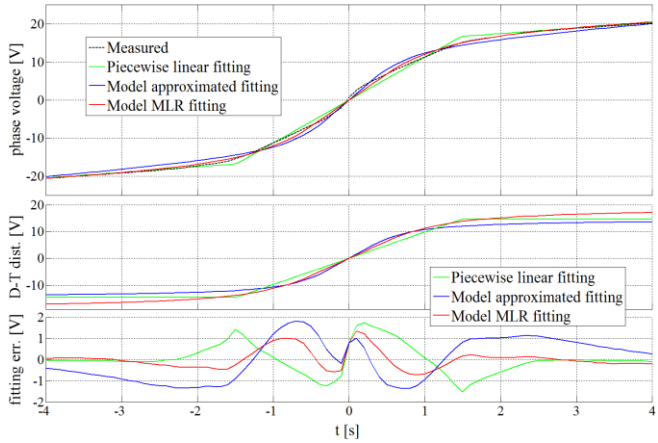



Fig. 7. Parameters identification procedure (acquired samples).

frequency could be increased, which would again increase the distortion effect. Even for the switching frequency and DC-bus conditions discussed above, 1 µs dead-time results in a maximum phase voltage distortion of about 7.5 V. While this may seem a small value, it is very close to the back-EMF amplitude of the 8-poles 2.8 kW SM-PMSM considered in the following, when running at 90 rpm (i.e. 3% of the nominal speed). Any back-EMF based sensorless technique would be ineffective under these conditions (and at slightly higher speeds, too), if proper compensation is not adopted. Also in cases other than sensorless control, such as where high-accuracy torque control is required, improved compensation reflects in better performances.




(a)




(b)

Fig. 8. Parameter identification procedure: phase voltage fitting (short (a) and long (b) motor connection wires).

Fig. 7 shows inverter distortion model parameter identification procedure, i.e. the acquisition of reference voltage and current samples. A staircase shape current reference is imposed to the $\alpha$ axis ($a$ motor phase), while the $\beta$ axis current is kept at zero. The corresponding voltage references for phase $a$ (current regulators output after inverse Park and Clarke transformations) is shown in the top diagram of Fig. 7.

One can notice the shape of the voltage is similar to that already shown in Fig. 5 in the theoretical analysis section, since current is incremented almost linearly (staircase). Acquisition of filtered voltage and current samples is done after the end of the transient related to the steps in current reference, which explains the small number of points in the figure.

For the same inverter and motor, two cases of distortion model fitting are shown with short (3m, Fig. 8a) and long (about 50m, Fig. 8b) motor connection wires. The two conditions show different distortion curves, which can be mainly explained by the different capacitance introduced by the cable. For the sake of comparison, different state-of-the-art techniques have been tested. The first (green) uses a linear-saturated model, [6], while the second (blue) used the physical model with approximated fitting [2], and the third (red) implements the MLR method proposed in this paper. For each method the top diagram reports the complete fitting (i.e. comprising resistive voltage drop), the middle one shows the distortion curve, while the bottom one represents the fitting error (i.e. the difference between the fitted and measured curve).

MLR regression only shows significant error around zero current, while for other techniques a sensible error is present all over the range. With the short cable, maximum error obtained by MRL is about 0.9V (while it is 1.4 for linear-saturated and 1.1V for approximated fitting). For the long cable case, MRL error is less than 1.3V (about 1.7V for linear-saturated and 1.8V for approximated fitting). It is worth noticing that this error values are very small if compared to the full-scale value for PWM generation, i.e. $V_{DC}$, representing less than 0.4%. In the short cable case, fitting error with the proposed method is about 0.16%.

Direct evaluation of the accuracy of the proposed compensation strategy is shown in Fig. 9, where a standard induction motor is used as a load and constant voltage amplitude and frequency are imposed, i.e. 10V peak at 4Hz. Four different conditions are considered (top to bottom): with no compensation, adopting a standard technique (linear and saturation distortion model), with the physical model fitted with the approximated method, and using the present proposal (MLR fitting on the physical model).

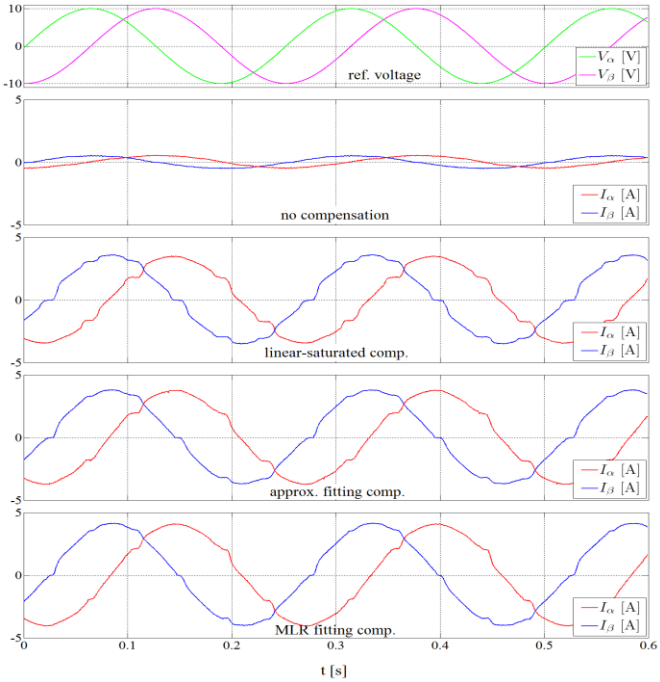



Fig. 9. Current distortion under sinusoidal voltage reference (10V, 4Hz).

A particular condition appears in the non-compensated case, where currents are almost sinusoidal (yet very low, with respect to the other cases). This is easily explained by considering the fact that, according to the model, at very low-current the dead-time distortion behaves linearly with current, i.e. as a high resistance, whose value depends on capacitance. All of the three compensation techniques achieve good results, but a slight increase in the current waveform quality can be observed from the first to the last method. This is also confirmed after calculation of the Total Harmonic Distortion (THD) of current, which decreases from 6.1% for the standard technique to 5.3% for the approximated fitting and 3.8% when MLR fitting is applied (considering up to the 25$^{th}$ harmonic).

A test was also carried out in the dual condition, i.e. under current control, with a 4A current space vector rotating at 4Hz, Fig. 10. Without any compensation (top diagram) the voltage reference shows a large distortion and the amplitude is much larger than in the compensated cases (since a first-harmonic component is present in dead-time distortion). Compensation is improved moving from linear-saturated compensation (second diagram), where THD is about 3.6%, to the approximated fitting (third diagram), where THD is 2.7% and finally MLR fitting, where THD reaches 2.6%.

An indirect verification of the accuracy of the compensation strategy was also obtained by considering a sensorless PMSM drive based on a back-EMF observer and analyzing the performances achieved in low-speed conditions. This operating condition is in fact heavily affected by the quality of the estimated back-EMF components that, in turn, strongly depends on the accuracy of the inverter voltage distortion compensation. The results are shown in Fig. 11, where the estimated $\alpha\beta$ back-EMFs are reported for the same four cases. The reduction in distortion level introduced by compensation is clearly visible from the reported waveforms. The proposed method (bottom diagram) achieves the lower THD (3.0%), while it becomes 3.1% using the approximated fitting and 3.9% with the linear-saturated curve.

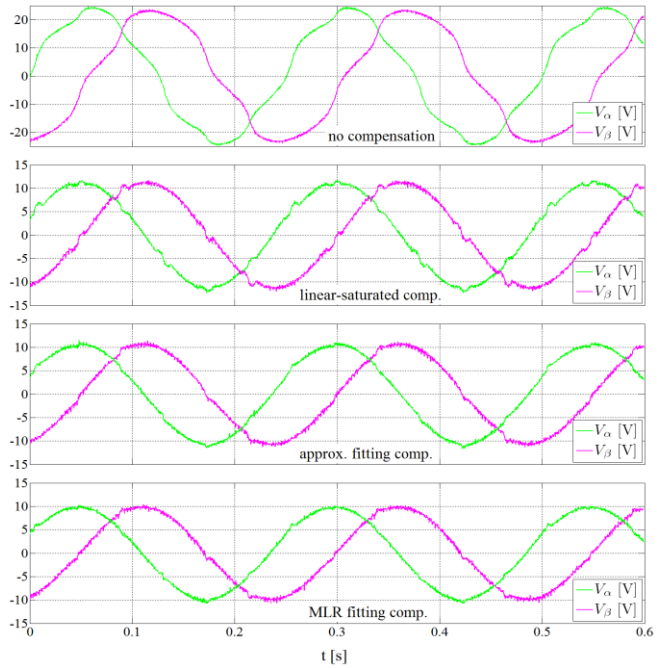



Fig. 10. Voltage distortion under sinusoidal current reference (4A, 4 Hz).

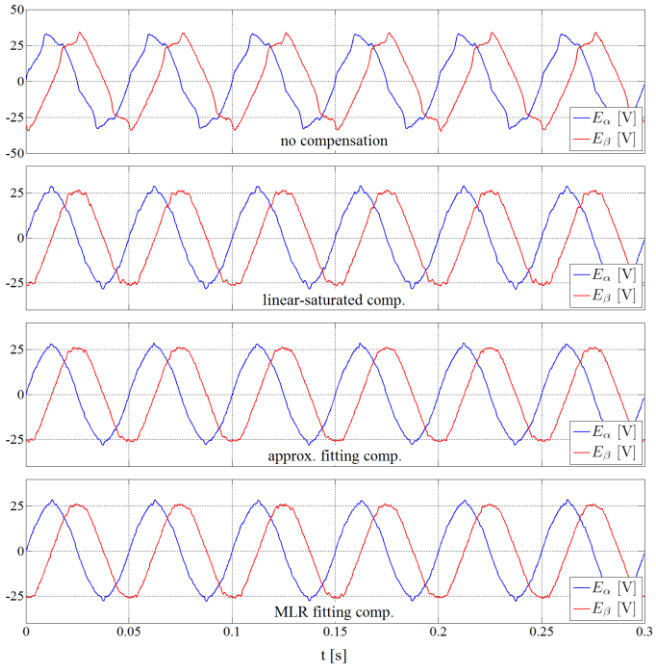



Fig. 11. Sensorless operation: back-EMF estimation at 20 Hz.

TABLE I. COMPARISON OF DEAD-TIME COMMISSIONING AND COMPENSATION STRATEGIES.

| Technique / Aspect | **LUT** [8] | **Piecewise linear** [6] | **Voltage measurement** [4] | **Harmonics based** [2][6][7][13][14] | **Proposed** |
|---|---|---|---|---|---|
| **Compensation complexity / computational cost** | Simple (requires LUT interpolation) | Simple | Simple, but requires very high-speed processing | Complex, relies on constant frequency behavior | Simple |
| **Commissioning complexity** | Simple, but memory consuming | Simple (straight-line regression) | Simple | Feedback stability not addressed | Medium-low |
| **Additional hardware with respect to a standard one** | None | None | Very fast ADC and processing (FPGA/MCU with DMA) and analog front-end (usually isolated) | None | None |
| **Accuracy** | High | Low | Strongly depends on time-base resolution (i.e. sampling rate) | Low: only works at steady-state and on certain harmonics | High |
| **Adaptation to DC-bus voltage and switching frequency** | No | Usually not included | Implicit | Implicit | Both parameters included in model |
| **Sensitivity to measurement noise** | Both commissioning and compensation prone to current measurement offset | Both commissioning and compensation prone to current measurement offset | Voltage measurement noise directly affects compensation | Low, but could be affected by other sources of distortion | Robust commissioning, compensation could suffer from current measurement offset |

## VI. CONCLUSIONS

This paper presents a novel self-commissioning technique for inverter voltage distortion identification based on a physical model of the power converter, including output parasitic capacitance effects. The unknown distortion model parameters are identified together with phase resistance at stand-still, adopting Multiple Linear Regression fitting. Improvements in identification accuracy and related advantages in motor control have been demonstrated with respect to standard techniques and state-of-the-art methods. A qualitative comparison is reported in Table I, where different aspects are considered, such as complexity, hardware requirements and accuracy.

Implementation of the proposed method on a general-purpose industrial drive is straightforward as it requires minimal amount of memory and computational resources.

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